Microcontroller–Based Modified SEPIC Converter for Driving Lamp with Power Factor Correction

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Abstract-A methodological study of electronic ballast for electrode less lamps including design and development issues is presented in this paper. The ballast is intended to feed a 300 W ultra violet lamp at 100 kHz with dimming feature. The proposed topology is composed of a Single-Ended Primary Inductance Converter (SEPIC), used as power factor correction (PFC) stage, integrated with a resonant half-bridge inverter, used as lamp power control (PC) stage. The integration of both stages is proposed in this paper, in order to reduce the number of active switches, as well as to simplify the required driving and control circuitry for this application. The implemented topology attained very high power factor (0.9982), and low line current total harmonic distortion (THD) (1.86%), without using electromagnetic interference (EMI) filter, while the measured efficiency was 90% at nominal lamp power.

Index Terms—**Ultra violet Lamps, Integration Technique, High Power Factor, High Switching Frequency.**

I. INTRODUCTION

In recent years, the power electronic systems and devices which are used more frequently create harmonics current and pollute the electricity network. Harmonics have a negative effect on the operation of the receiver, which is fed from the same network. Fig. 1 which should provide satisfactory lamp operation, fulfilling the standards of power factor (PF) and efficiency of the energy drained from the grid [1].The EMI filter is designed to eliminate the harmonic components generated by the high frequency switching of the PFC stage, because otherwise high frequency harmonics can decrease [2],

[3] the system power factor and cause interference problems with other equipments.
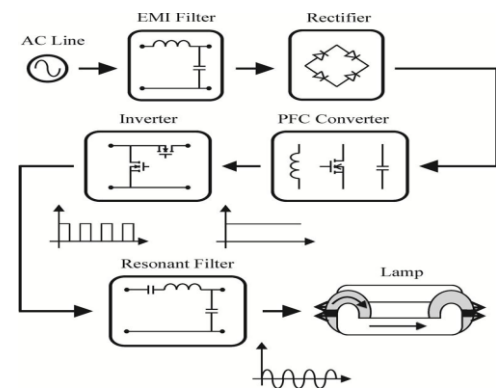

Fig.1. Operating stages of an EFL drive

In this paper, an integrated converter that incorporates both the PFC and the PC stages is proposed. A methodology for achieving luminous flux control in this type of integrated converters is also investigated. For the PFC stage a SEPIC topology is employed, while for the PC stage a half-bridge resonant inverter is used [3]. Both of them will operate at the same switching frequency (fs) given by the lamp requirements. The proposed converter is then intended to drive an EFL type 300 W from Osram operating at 100 kHz. Electrical, built and lighting features of this lamp are presented in [7] and [8].

II.SEPIC –CONVERTER

This paper proposes the integration of the PFC and the PC stages, in order to reduce the number of active switches, as well as their respective control circuits. The integration technique is the combination of two controlled switches in a single one. As a

condition, both switches must have at least one common node [4]. One limiting factor of the integration technique is that both stages, PFC and PC, being integrated will have the same switching period (*Ts*) and duty cycle (*D*) imposed on the shared switch. After the integration, each stage will keep its own characteristics independently, as if there were no circuit components sharing [11]. Fig. 2 shows the proposed topology in its non-integrated form. Fig. 3shows integrated topology. As commented previously, it is made up by a SEPIC as PFC stage and a half bridge resonant inverter as a PC stage.

A. PFC stage

The SEPIC is suitable to be employed as a PFC stage and output voltage regulator in the proposed topology. This converter [5] is attractive because it operates as a voltage step-down or step-up stage, depending on the imposed duty cycle. Another advantage is that the output voltage has the same polarity as the input voltage, thus simplifying control and protection circuitries. The Fly back PFC topology may also be considered as an alternative to feed the half-bridge inverter. One of the features of this topology is the insulation between input and output. However, when applied to the integration technique, the Fly back topology intrinsic insulation no longer takes place. In this way, the Fly back topology resembles to the Buck-Boost topology where leakage inductances and core size are reduced. The non-inversion [14] of the output voltage and the possibility of input filter elimination are some features that lead to the use of SEPIC PFC instead of Buck-Boost PFC Topology. In addition, if the input inductance used in the SEPIC (*L1*) is high, the line current will present inherently low ripple, thus requiring small EMI filter components that, in some cases, may be eliminated. This reduces the number of stages, increases efficiency and decreases cost [10].
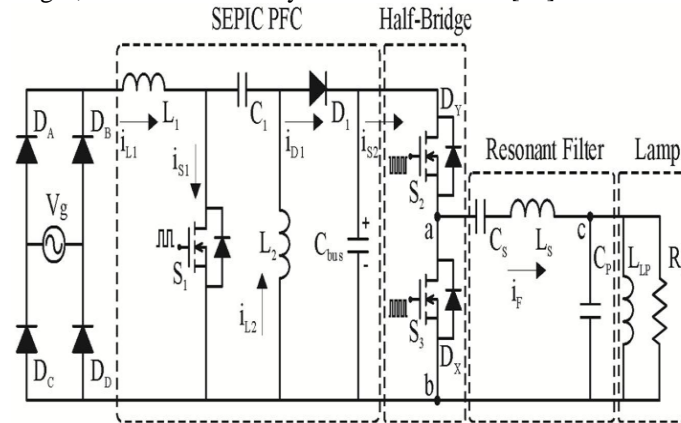

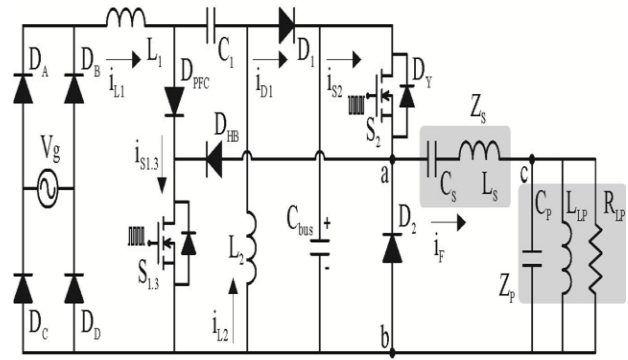Fig. 2 Non-integrated electronic ballast.

Fig. 3 Proposed single-stage SEPIC half-bridge EFL integrated electronic ballast.

The SEPIC can be operated in continuous conduction mode (CCM) and/or discontinuous conduction mode (DCM). Given the low power level intended for the proposed application [2] (<300 W) and in order to simplify the control circuit, the DCM is chosen. In this way, the SEPIC operating in DCM with constant duty cycle and switching frequency behaves as a resistance to the AC line, thus assuring high input PF.

B. PC stage

The use of a high-frequency half-bridge inverter, followed by a resonant filter, to perform the lamp starting and stabilization in steady state is consolidated in the literature [13].

The resonant load consists of a LCC filter, associated with the EFL electrical model. The operating frequency is given by the half-bridge inverter, which usually operates, near the filter resonant frequency during starting process. The resonant filter is used to adapt the square waveform supplied by the inverter, attenuating the high-order harmonic components and supplying the lamp with sinusoidal waveforms [12]. A number of criteria must be considered when designing this circuit, so that the lamp can be satisfactorily driven. For example, the circuit must provide the required lamp ignition voltage and limit the current in steady state to its nominal value.

C. PFC and PC Stages

A high number of stages for feeding the lamp involves a more complex topology, increases cost, decreases revenue and undermines the circuit reliability. Thus, the elimination and/or integration of these stages provide component reduction, making the system more attractive. The integration of DC-

DC converters [6] and DC-AC aims to reduce the number of controlled switches, which also implies the use of a simpler control circuitry and cost reduction. In the proposed topology, the integration takes place between the switches □□and □□ shown in Fig. 2, resulting in the SEPIC half-bridge circuit, as shown in Fig. 3. This integration is known as *T* type [7]. In this type of integration, the shared switch must handle the current sum of both stages. Thus, the shared switch does not present overvoltage. The switch *S1.3* drain-source voltage is equal to (*Vpk + Vbus*), which is intrinsic to the SEPIC PFC topology. Diodes *DPFC* and *DHB* are used to prevent undesirable circulating currents from one stage to the other (PFC and PC stages).The diode *D2* is equivalent to the intrinsic diode of switch*S3* in the non-integrated topology. The voltage and current efforts over this diode are the same before and after to apply the integration technique.

D. Operation Stages

In this section, the operation stages of the SEPIC half bridge converter are presented. In the analysis, the resonant filter current is considered sinusoidal and the semiconductors are considered ideal switches.

Stage 1 (t0 – t1): In this stage, switches *S2* and *S1.3* are off. The SEPIC is in its freewheeling interval, current *iL1* being equal to -*iL2*. The resonant current (*iF*) flows through diode *D2*.

Stage 2 (t1 – t2): In this stage switch *S1.3*, is turned on and switch *S2* is off. In the SEPIC, *Vg* is applied to the input inductor *L1,* while the voltage across capacitor *C1* is applied to inductor *L2*. In this stage, the resonant current circulates through diode *D2* and switch *S1.3* is subjected only to the SEPIC current. This stage ends when the current through diode *D2* reaches zero due to the inversion of the resonant current.

Stage 3 (t2 – t3): In this stage, *S1.3* is conducting, diode *D2* is off and the resonant current circulates through diode *DHB* and switch *S1.3*. In the SEPIC topology, *L1* and *L2* are still being energized by the input voltage and *C1* capacitor voltage respectively.

Stage 4 (t3 – t4 – t5): In this stage *S1.3* is turned off. In the half-bridge inverter, the resonant current circulates through the body diode of switch *S2* (*DY*). In the SEPIC the inductors *L1* and *L2* are de-energized by the voltage across capacitor *Cbus*.Both inductances and resonant circuit supply current to the *Cbus* capacitor. In this stage, *S2* is turned on;

however the resonant current circulates through the body diode of *S2,* so the switch *S2* is turned on with zero voltage, thus achieving zero voltage switching (ZVS).

Stage 5 (t5 – t6): In this stage, *S2* is conducting. The Resonant current reverses and begins to circulate through switch *S2*.

Stage 6 (t6 – t7): In this stage, diode *D1* current reaches zero, characterizing the DCM operation. The resonant current circulates through switch *S2*. The SEPIC enters in freewheeling mode, where the current through inductors *L1* and *L2* are equal in magnitude (*iR*) and have the direction shown in Fig. 7(f). At the end of this stage, switch S_2 is turned-off, reaching stage 1 and repeating the process.

III ANALYSIS AND DESIGN OF THE SIMULATED PROTOTYPE

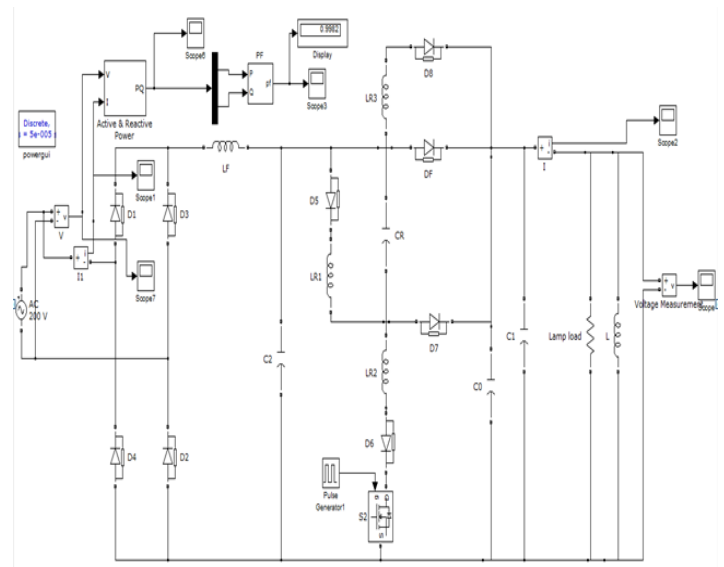MATLAB/Simulink model is used to simulate the proposed model.

Fig.4 Simulation Diagram of the Proposed System

The 230V AC input is given to the supply. The Bridge rectifier is used to convert AC to DC and given to the passive filter. Frequency can be fixed in the passive filter. So that output is given to the active filter which varies the frequency value and also it allows high voltage and current [15]. Here the input voltage is increased to 440V DC and converted to 440 AC by using converter. The Harmonics also reduced and the output is given to the ultra violet lamp.

IV. EXPERIMENTAL RESULTS

This section shows the experimental results of the simulated prototype. The results also show the buck and boost voltages according to the reference voltage.

Fig.5 Shows the AC input voltage given to the simulated prototype. Here applied AC voltage is 200V.
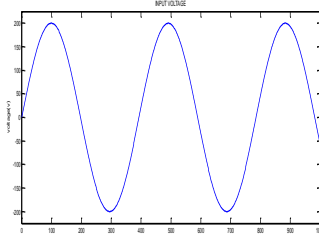

Fig.5 Input voltage

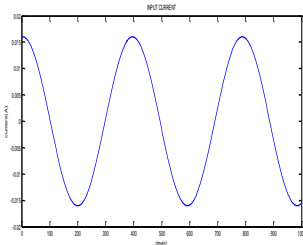Fig.6 shows the input current given to the simulated prototype. Here applied current is 0.016A.

Fig.6 Input current

Fig.7 shows the operated voltage with respect to reference voltage. The output voltage we obtained is 400V.
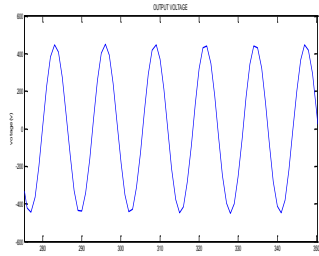

Fig .7 Output voltages

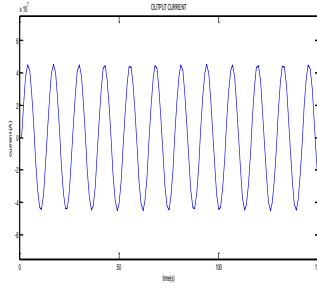Fig.8 shows the output current of the system is 4.2A

Fig.8 Output current

Fig.9 shows the power factor maintained by the device Equal to 0.9982.
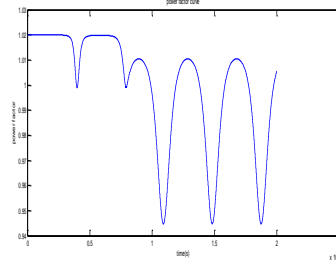

Fig.9 Power factor

Fig.10 shows the Real power and Reactive power of the device. Real power=50W, Reactive power=0W
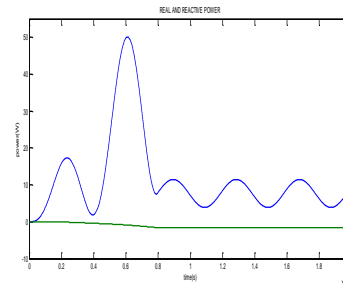

Fig.10 Real and Reactive power

V. CONCLUSIONS

This paper presented the SEPIC half-bridge integrated topology to feed an electrode less fluorescent lamp. Initially, important characteristics of ELFs were presented, as well as its electric model, necessary for the design of the integrated converter. The proposed circuit was designed for DCM operation, so that the converter could be represented as an equivalent resistance. Thus, a high system power factor was obtained, associated with a low THD, in order to optimize the energy drained from the AC line. The integration of the PFC and PC stage reduced the system component count. However, the

integrated switch should be designed so as to handle both efforts of circuit current and voltage. In spite of the stage integration, as well as high switching frequency required to supply the lamp and the absence of EMI filter the experimental, the results validated the proposed topology.

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